EXPEDITION ENTERPRISE

The technology leader for today's most complex PCB systems designs

Mentor Graphics®

A Tightly Integrated Systems Design Flow

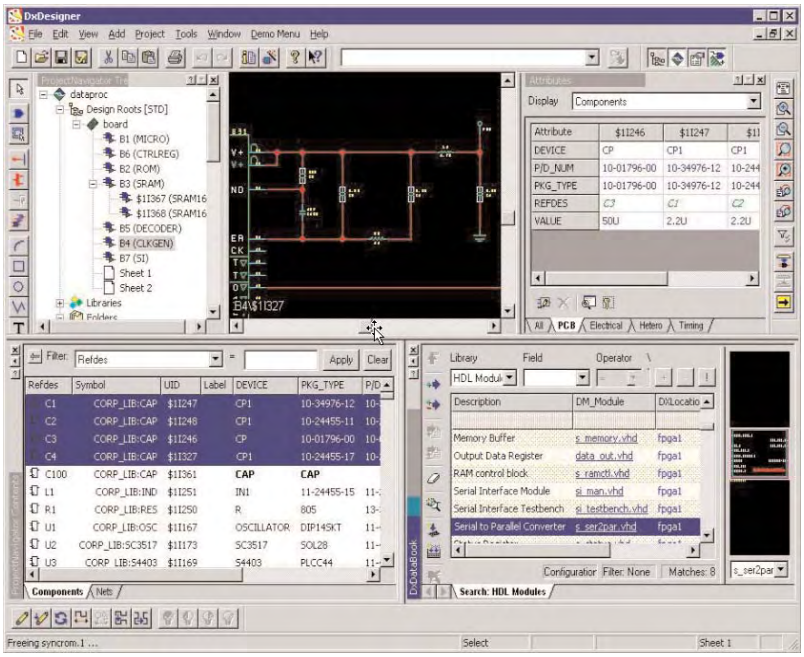
The Expedition™ Enterprise flow is well known for its advanced technology and capabilities for creating today's most complex PCB designs. However, it's Expedition's single, tightly integrated design environment and its ability to meet the needs of mid-sized to large electronics companies that really sets it apart from the competition. It features a common database, common user interface and rules that eliminate the burden of managing multiple tools to complete a design. Its electrical and manufacturing constraint management system, and design data and library management provides support for local or globally dispersed design teams to leverage their resources and reduce design cycle times. Data integrity is constantly maintained - from concept to manufacturing. Expedition's superior integration drastically reduces the time needed to complete ECOs and total design time, while eliminating costly errors.

Systems Design with Expedition Enterprise

When you're designing a product, you need more than just a great PCB layout tool - you need a tightly integrated design system. Expedition Enterprise provides this high level of integration, enabling all members of the design team to work more efficiently, thereby speeding up the design process.

Integration of Expedition PCB™ for layout with DxDesigner™ facilitates a seamless transfer of rules and cross-probing between the schematic and layout environments. As a project evolves from concept through to finished product, the database is always kept in synchronization, notifying the engineer and designer of changes as they occur and eliminating unnecessary and costly design iterations.

Expedition Enterprise is integrated with DMS™ (Data Management System), providing a central infrastructure for component libraries, design data versioning and management, design reuse, where used, and integration with corporate PLM systems. Once the design is complete, integration with manufacturing output tools ensures that the integrity of the design is maintained.



DxDesigner provides a complete solution for design creation, definition and reuse.

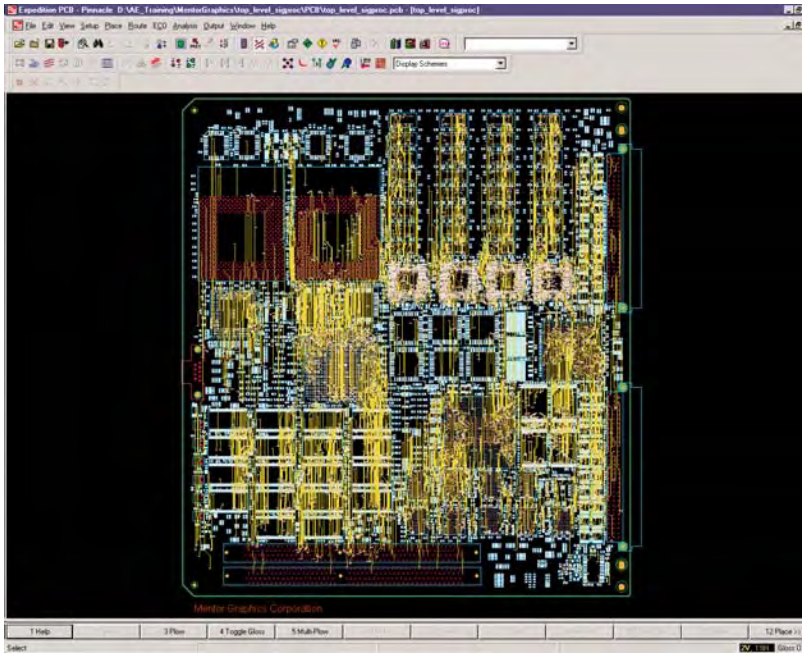
System Definition

DxDesigner provides a complete solution for design creation, definition and reuse. It provides everything needed for circuit design and simulation, component selection and library management, signal integrity planning, project management and team-based design. DxDesigner has the ability to publish schematics, library data and other design data through a web server, so that any user with the appropriate permissions can gain access to this information using a web browser. DxDesigner is also integrated with several product lifecycle management systems, making design data, PDF schematics, and BOMs available throughout the company. It also supports a centralized, Internet-based library so that only one version of the corporate library needs to be maintained.

Additional components include DxDataBook™ for centralized library access, DxPDF™ for creating a PDF schematic, DxVariantManager™ for variant design definition, DxDataManager™ for design file management and DxViewOnly™ for viewing schematics through a Web plug-in.

FPGA-On-Board Design Collaboration

To help with the growing demands of FPGA and PCB design, Mentor Graphics offers I/O Designer™, a fast and efficient solution for assigning the I/O of your FPGA to device pins in the PCB layout. I/O Designer integrates the FPGA and PCB design flows to provide top-down concurrent design of the FPGAs and the PCB so design teams can reduce design cycle time and optimize performance at the system



Expedition PCB is simply the most productive solution available for the creation of dense, difficult, high technology PCB designs.

level. By maintaining a library of parts for FPGAs from major vendors, I/O Designer supplies all of the important information about each pin of the selected device. Using this information, users can choose to assign all of the signals to pins on the device or only those signals deemed critical to the design. They can also assign I/O standards for those critical signals. In this way, the FPGA pin-out can be optimized prior to PCB layout to insure the best system performance, reduced PCB routing congestion and design cycle time. Do you need to swap pins on the PCB to improve the layout further? I/O Designer knows which pins are swapable and which are not.

I/O Designer also manages the consistency between the FPGA and PCB flows by acting as a data management tool, monitoring each flow and managing any changes that occur. Pin swaps carried out on the PCB are picked up by I/O Designer and the necessary files updated. I/O Designer then generates FPGA place and route constraints, based on the HDL design and pin I/O assignment process, and creates the necessary symbols, schematics and hierarchical associations based on the "post route" pin data.

PCB Layout

Expedition PCB for layout, powered by AutoActive® technology, is an integral part of the tightly integrated flow. By combining ease-of-use with advanced functionality, Expedition PCB offers designers the leading technology for the creation of today's most complex designs. It includes interactive and customizable multi-pass autorouting controls for design challenges, such as differential pair routing, net tuning, manufacturing optimization and microvia and buildup technology.

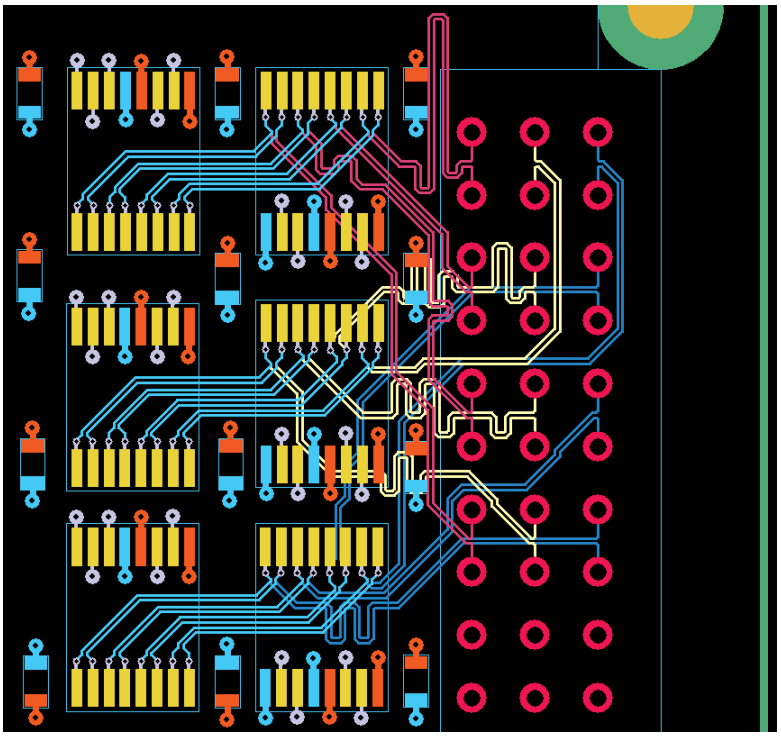
AutoActive - The Technology Leader in PCB Design

AutoActive technology represents a revolutionary step forward for PCB design. The power of industry-leading autorouting technology is combined with interactive editing capabilities to produce a single, powerful and easy-to-use design environment. This environment eliminates the burdens of jumping between tools to get the job done and managing differences between the constraints on the autorouter and on interactive editing.

AutoActive provides designers with greater control than ever before, with the ability to easily switch between automatic and manual editing as needed. From simple tasks, such as defining board areas, to complex procedures that involve maintaining high-speed signal conditions, all objectives are accomplished with the system and the designer working together in real-time. The net result of AutoActive technology is reduced design times, increased productivity and unmatched design quality.

What is AutoActive?

- A single, integrated, place and route editing environment that reduces total design time and increases productivity.
- All physical rules and high speed rules are maintained.
- Correct-by-construction design that produces high-quality results with clean-up time eliminated.
- Shape-based, true 45 degree routing.
- The most advanced autorouting technology ever. Stop and start the autorouter at any time and all results will be correct-by-construction.
- Dynamic clean-up of traces through the reduction of segments, prevention of acute angles, and application of pad entry rules.



Routing and editing differential pairs with Expedition PCB is accomplished with speed and ease that will change your view of high-speed design.

Dynamic Area Fills

Expedition PCB automatically clears area fills around traces, vias and pads as the board is edited. Dynamic area fills are so fast, it allows users to keep their area fills turned on while they are doing all necessary edits. Moving a via pushes and shoves other vias, traces and area fills and connectivity is automatically maintained.

Rules By Area

The rules by area functionality greatly improves routing around BGAs and other fine-pitched parts. Rule areas represent complete rule sets that are obeyed by online and batch DRC and in interactive and automatic routing. Rule areas may be defined by layer and can be assigned to any polygon, rectangle or circle. Trace widths and clearances automatically change when traversing into or out of the rule area. Designers may also change via sizes and spans in a rule area to maximize route completion.

Multiplow With Variable Via Patterns

Expedition PCB's multiplow functionality allows designers to simultaneously route multiple nets, including differential pairs, with true 45 degree routing. It can even handle routing through areas of staggered pins. Traces being routed push and shove the other vias and traces out of the way and automatically clear area fills as needed. Changes can be easily made to a variety of selectable via patterns at the touch of a button, allowing enhanced flexibility for routing into dense areas of a design.

Dynamic Hazard Review

Design hazards are dynamically displayed and may be individually selected and colored for easy identification. When a hazard is fixed, it is dynamically removed from the hazard list.

Engineering Change Orders

ECOs can cause delays and introduce errors in the design process. The Expedition Enterprise flow makes ECOs less painful and more accurate than ever before. In addition, Expedition PCB's powerful automation and tight system integration drastically reduces ECO completion times and eliminates synchronization errors. Designers can change rules, replace parts and reroute automatically with no rule violations, all in real - time.

High-Speed Layout

Designers today are increasingly challenged by the need to manage signal quality in order to achieve system performance and reduce prototype iterations. High-speed design with Expedition PCB is an integrated part of the AutoActive design environment.

Constraint Definition

Expedition PCB for layout handles an extensive set of constraints to meet high-speed performance requirements whether they're routed interactively or automatically. The Constraint Editor System™ (CES) provides a fully integrated, constraint-driven design methodology that reduces design costs and time-to-market by automating the communication of design rules and eliminating unnecessary PCB prototypes and re-spins. CES provides common constraint entry for electrical and physical high-speed rules. CES has an easy-to-use spread-sheet-like GUI guided by the design database with cross probing tothe schematic and layout.

- Rules are preserved on net re-names, connectivity additions/removals, pin and/or gate swaps and stackup changes.
- The GUI offers easy differential pair creation, parallelism rules entry and pin-pair creation.

- Hierarchical constraint entry enables simple assignment of complex topologies with filtering and sorting.

Net Tuning

While routing interactively, graphic tuning aids are displayed for guidance. Nets modified out-of-tune during edits are automatically re-tuned. The Hazards dialog box dynamically updates as users edit nets, providing instant feedback relative to their constraints. Nets can also be tuned automatically within an autoroute pass. Tuned nets are automatically maintained as the designs are completed.

Differential Pair Routing

Routing and editing differential pairs with Expedition PCB for layout is accomplished with speed and ease that changes the view of high-speed design. Pair spacing rules can be established by both layer and net class. If one trace is edited, the other trace in the pair automatically moves with it. Adjacent layer differential pair routing capabilities add another valuable option for routing critical signals on a dense PCB.

Simultaneous Design

XtremePCB™ is a revolutionary and exciting new technology that enables multiple PCB designers to work on a single design database simultaneously over LAN or WAN networks. Unlike traditional team design methodologies that employ a split-and-join approach to design collaboration, XtremePCB requires no physical partitioning and every designer sees all other client edits in real-time. Because no further training or complex setup is required, designers can be brought in at any time and from anywhere in the world to collaborate on time-critical projects, dramatically shortening design cycle times. It is ideal for large, complex designs or PCBs with mixed technology where specialists need to focus on their part of the design.

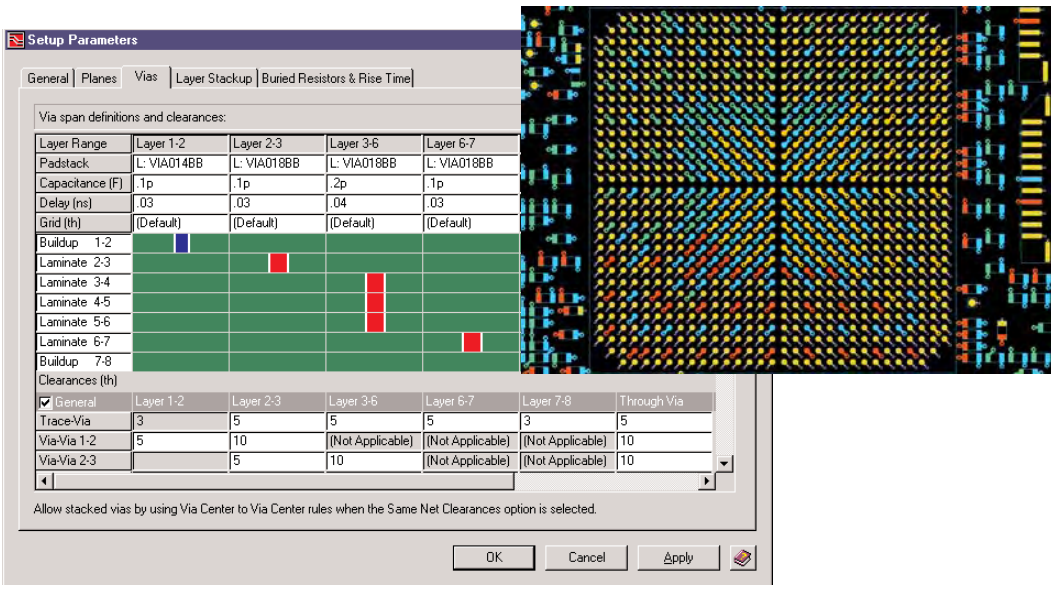
Team Design

TeamPCB™ also allows multiple designers to work on the same PCB layout design. Through a process of partitioning in the layout design phase, today's design teams can "divide and conquer" projects in a fraction of traditional schedules. Traditional team design and concurrent design methods relied on logical partitioning or design reuse blocks, which often involved the error prone manual editing of ASCII files and databases. TeamPCB eliminates many problems associated with other team design processes, through an automated design methodology that manages all edits and keeps design files synchronized.

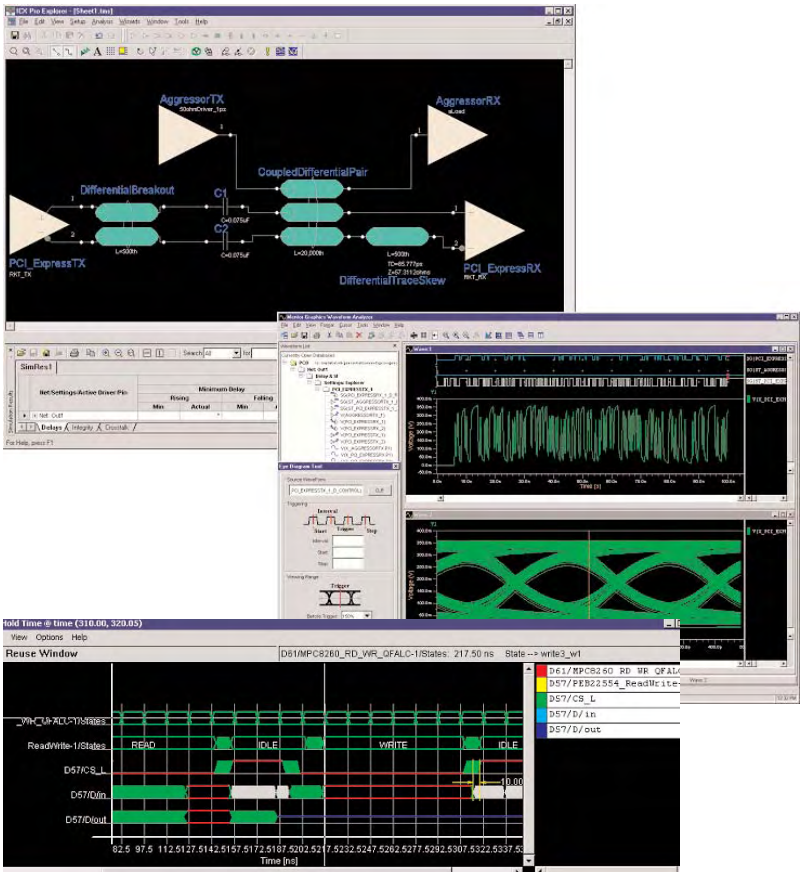
Advanced Interconnect Routing

The challenges and solutions of advanced interconnect are prevalent today with BGA, CSP, COB and DCA packages increasing board density. Build-up and microvia structures used in these board designs further complicate routing. Expedition PCB offers the leading technology for advanced interconnect designs.

It supports the definition of complex



Expedition PCB offers the leading technology for the creation of advanced interconnect designs.



With Expedition Enterprise, timing and signal integrity issues can be addressed and corrected throughout the design process rather than just at the end.

via structure rules and the routing of microvia geometries, including routing under pads. Via spans between any two layers are possible. By moving beyond traditional laminate layer pairing, Expedition PCB facilitates the design of build-up structures on laminate to enable escape patterns from dense, high pin count devices. Build-up areas typically have a smaller clearance than the laminate beneath them. Expedition PCB can establish delay values and clearances per via span to address these issues. Additionally, it features true 45 degree routing for BGA fanout and staggered connectors, enabling localized rule definition to facilitate escape paths from dense areas.

Design Reuse

The Design Reuse module creates and stores reusable blocks of circuitry, including schematic and PCB placement and routing data, in a central library. These blocks can then be placed and modified within the same design and across multiple designs. Design reuse automates this process and manages the design data to ensure error free databases and reduce the overall PCB design cycle time.

Variant Management

Variant Manager manages the creation of multiple product configurations from a single design database. Variant Manager's single-point ECO management minimizes errors, reduces costs, improves design quality and enhances production efficiency.

RF Circuit Design

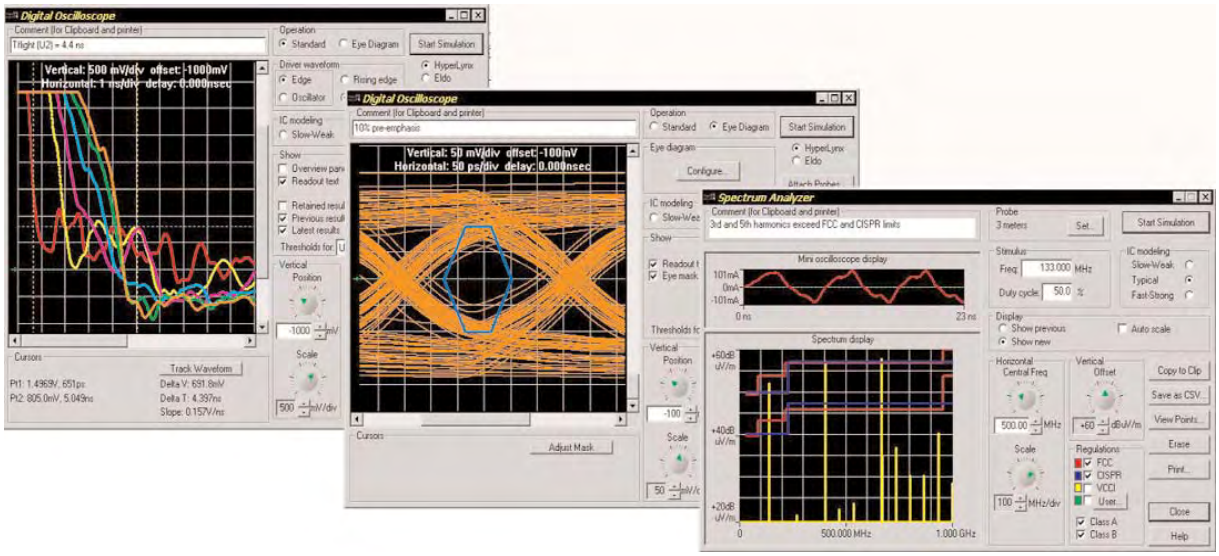
Many PCB designs, such as cell and handheld phones, incorporate RF circuitry. RF layout design and simulation is a specialized function that is generally carried out in dedicated point tools. With the IFF/Agilent ADS Interface, RF data that is designed, simulated and verified in Agilent's ADS product can be directly imported to and exported from DxDesigner and Expedition PCB, ensuring that the databases are synchronized and data integrity is maintained.

Signal Integrity, Timing Analysis and EMI

With the Expedition Enterprise flow, timing, signal integrity and electro - magnetic interference (EMI) issues can be addressed and corrected throughout the design process rather than just at the end. This ensures that designs are correct the first time, effectively reducing design iterations and creating the opportunity for optimum system performance.

The enterprise high-speed solution is centered around the common CES and ICX™'s powerful simulation technology. ICX Pro Explorer™ allows users to evaluate high-speed requirements and produce constraints to drive the design flow. The flexible model support (IBIS, SPICE, S-Parameter and VHDL-AMS) allows users to simulate both traditional parallel buses and the evolving high-speed serial architectures. The schematic-like view of the design data simplifies the task for the electrical engineer and allows constraint templates to be generated for use on both current and future designs.

Constraints generated from ICX Pro Explorer are used within the Expedition Enterprise flow to drive the placement and routing of the design. The same constraints and model information used



HyperLynx enables powerful, easy to use signal integrity, crosstalk, and EMC analysis prior to layout, after component placement, and after a board has been fully routed.

in ICX Pro Explorer are used at both the design and system level for exhaustive, final electrical verification in ICX. The addition of Tau® to the flow allows timing verification to be carried out at any stage. Tau's symbolic timing analysis approach addresses the limitations of traditional static timing tools, by eliminating the identification of large numbers of false paths. The combination of both electrical and physical constraints driving layout with access to common model information and advanced simulation technology provide a best-in-class, integrated high-speed design flow.

In addition to the enterprise high-speed solutions, HyperLynx® provides pre- and post-layout signal integrity, crosstalk and EMC analysis for traditional high-speed interconnects, as well as the emerging serial and multi-gigabit-per-second SERDES technologies. HyperLynx's easy to learn analysis environment makes it an every-desktop standard for Expedition Enterprise.

Of increasing importance due to higher frequencies and government regulations is the elimination of electromagnetic interference. This normally required the production of a prototype board, testing in a shielded chamber and re-design. Now with Quiet Expert™, the causes of EMI can be highlighted and eliminated during the design layout thus significantly reducing design iterations and saving valuable time-to-market.

System Verification

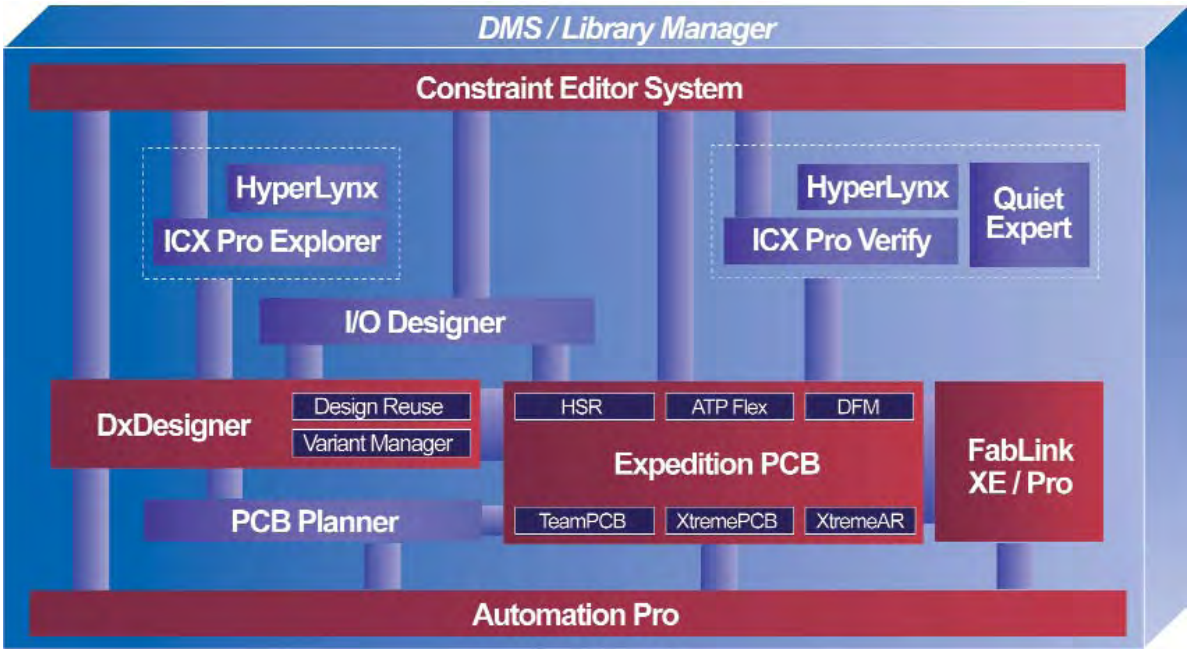
DxAnalog™ verifies analog and mixed analog/digital designs at the system or board level. It is tightly integrated into DxDesigner and combines ease-of-use with powerful simulation, preparation of stimuli, and complex analysis of circuits and verification through graphing and output.

ModelSim® is the world's most popular and widely used VHDL and mixed-VHDL/Verilog simulator and the fastest-growing Verilog simulator. ModelSim products are uniquely architected using technology such as Optimized Direct Compile for faster compile times and simulation performance, Single Kernel Simulation (SKS) and Tcl/Tk for greater levels of openness and faster debugging. Exclusive to ModelSim, these innovations result in leading compiler/simulator performance, complete freedom to mix VHDL and Verilog and the unmatched ability to customize the simulator.

Manufacturing Preparation

Manufacturing and fabrication have always been an extremely integral part of PCB design. Previously, designers had to use multiple applications to create schematics, layouts and prepare designs for manufacturing. To make the process easier, Expedition Enterprise has Fablink XE™, an integrated manufacturing data creation, generation and verification environment powered by AutoActive. Fablink XE was created specifically for designers to control their fabrication data at either the board or panel level, thus ensuring design and manufacturing data integrity.

Fablink XE provides a stand alone panel creation and editing environment for creating manufacturing data at the panel level that operates on a panel design database. In addition, it provides



The Expedition Enterprise flow addresses the needs of the mid-sized to large enterprise electronics company.

additional board level functionality, including detailed data views, searchable PDF output, copper balancing, various data outputs and Gerber In/Drill In capabilities.

The Design for Fabrication (DFF) functionality performs critical fabrication rules checking during the design process to eliminate costly design respins due to last minute errors discovered in manufacturing.

Library, Design Data Management and Enterprise Integration

In today's world of tighter regulatory controls over use of hazardous substances, increased use of global manufacturing, greater reliance on third parties for both design and manufacturing and all combined with more complex designs, the need for better tools to help manage the design process and to achieve a tighter linkage between design and enterprise business systems has never been greater.

DMS brings the electronic design process to the supply chain, and brings the supply chain to the designer's desktop. It ensures complete data consistency, accuracy and availability throughout the design enterprise. Additionally, DMS consolidates multiple data systems, enabling collaboration and life cycle management across multiple team members, disciplines and sites.

It does this by integrating design data management with component information so that corporate component procurement policies (approved parts, preferred vendors) are easily available on the desktop. This helps designers to make optimum component choices and to manage parts lists during the design process so they can be released as accurate BOM's that meet corporate policies for cost, reliability and regulatory compliance. At the end of the project, DMS manages the release process so that accurate product documentation can be transferred to enterprise manufacturing, PLM and ERP systems, and supply chain management systems.

Support, Education and Consulting

Mentor Graphics offers a full range of services to drive your productivity and success with the Expedition Enterprise flow tools. Customer Support offers award-winning technical assistance, innovative electronic support and high-quality product enhancements. Education Services offers classroom and online training to help you assimilate new tools and technologies into your design environment. Finally, Mentor Consulting is always ready to provide focused expertise in tough design areas.

Hardware Requirements

- Pentium® III or higher
- Memory: 256 MB RAM

OS Requirements

- Windows XP Professional, HPUX, Sun OS and RedHat Linux

Systems Design Division
Mentor Graphics Corporation
1811 Pike Road
Longmont, CO 80501
720.494.1000 Main
888.482.3322 Sales
www.mentor.com/pcb

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
503.685.7000 Main
800.547.3000 Sales
www.mentor.com

JC-09-05 1020860